REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the subject application. The Office Action of December 4, 2002 has been received and contents carefully reviewed.

Claims 12-20 are currently pending. Claim 12 has been amended for clarification. By these amendments, Applicants do not acquiesce to the propriety of any of Examiner's rejections. These amendments, therefore, do not disclaim any subject matter to which the Applicants are entitled. *Cf. Warner Jenkinson Co. v. Hilton-Davis Chem. Co.*, 41 USPQ2d 1865 (U.S. 1997). Indeed, these amendments are made merely to clarify the subject matter therein, as discussed in detail below. Reexamination and reconsideration are respectfully requested.

In the Office Action, the Examiner rejected claims 12-20 under 35 USC § 102(e) as being anticipated by Terasaka et al. (US Patent No. 6,335,492). Applicant respectfully traverses this rejection.

Claim 12 is allowable at least for the reason that claim 12 recites a combination of elements including forming a first layer above the transparent substrate to cover at least a portion of the transparent substrate, wherein the first layer exposes the pad of the each line and defines at least one opening near the pad, the opening having a depth lower than the surface of the first layer; and forming a second layer having a first part and a second part, wherein the first part is affixed to the pad to provide an electrical signal to the line and the second part is affixed to a bottom surface of the opening defined in the first layer to enhance adhesion between the first and second layers.

Although the grounds of the rejection appear to be different, Applicant submits that none of the cited references teaches or suggests each and every feature of the claims.

In Terasaka et al., a tape carrier package with terminals is provided wherein element

18/52 is a printed circuit board, elements 27/40 and 34/50 are connecting terminals, element 24/32 is an anisotropic conductive film having conductive particles therein, and element 54 is an adhesive such as epoxy resin.

First, the printed circuit board in the reference is clearly not a transparent substrate. One difference between an amorphous silicon (a-Si) thin film transistor (TFT) process and a crystalline silicon (c-Si) or "non"-TFT semiconductor process is that a semiconductor layer is deposited onto a glass substrate in an a-Si TFT process, while Si wafers are used as the substrate in a c-Si "non"-TFT semiconductor process. Although it is not clear which process is used to form base film 20/42, the element referred to by the Examiner as a "substrate" is clearly not of the type of substrate used in liquid crystal display devices.

The Examiner refers to the connecting terminals as lines, but again, when referring to a liquid crystal display device, the terminology "lines" are meant to describe gate and source lines, for example.

Next, the Examiner refers to element 48 as a first layer, and elements 46' and 54 as the second layer, however, copper portions 46' are coated by element 48, which is a tin-coated layer, and element 54 is an adhesive coating. The cited reference does not teach a first layer that covers at least a portion of a transparent substrate, exposes the pad of each line and defines at least one opening near the pad, the opening have a depth lower than the surface of the first layer. The cited reference does not teach a second layer having a first part affixed to the pad and a second part affixed to a bottom surface of the opening defined in the first layer. The alleged openings between terminals 50 in the reference do not have a part of either elements 28, 32, 46' or 54 affixed to a bottom surface of the alleged openings.

Applicant respectfully requests that the rejection under 35 USC § 102(e) be withdrawn. Moreover, claims 13-20 are allowable by virtue of their dependence on claim 12, which is believed to be allowable.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Applicants believe the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited. Should the Examiner deem that a telephone conference would further the prosecution of this application; the Examiner is invited to call the undersigned attorney at (202) 496-7371.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136. Please credit any overpayment to deposit Account No. 50-0911.

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Respectfully submitted,

By _____
Teresa M. Arroyo
Registration No.: 50,015

MCKENNA LONG & ALDRIDGE LLP
1900 K Street, N.W.
Washington, DC 20006
Telephone: (202) 496-7500
Facsimile: (202) 496-7756
Attorneys for Applicant

Version With Markings to Show Changes Made

In the Specification

Please amend the specification as follows:

Page 1, line 3:

The present invention relates to a method for manufacturing a liquid crystal display (LCD) device, and in particular, the present invention relates to a method for an LCD in which the pad terminal communicating [the electric] an electrical signal [with the] to an outer device and the terminal of the outer device [are cohering] cohere well with each other, and to the structure of an LCD having the same pad terminal.

Page 2, line 20:

The lower panel 5 of the LCD comprises switching elements and bus lines generating the electric field for driving the liquid crystal layer. This panel is called an active panel. The active panel 5 of an AMLCD includes pixel electrodes [47] 41 designed in a matrix pattern and formed on a second transparent substrate1b. Along the column direction of the pixel electrodes 41, signal bus lines 13 are formed, and along the row direction of the pixel electrodes [47] 41, data bus lines 23 are formed. At a corner of a pixel electrode [47] 41, a TFT 19 for driving the pixel electrode [47] 41 is formed. A gate electrode 11 of the TFT 19 is connected with the signal bus line 13 (or the gate line). A source electrode 21 of the TFT 19 is connected with the data line 23 (or the source line). A semiconductor layer 33 is formed between the source electrode 21 and the drain electrode 31. [The] An ohmic contact exists between the source electrode 21 and the semiconductor layer 33 [are ohmic contacted to each other.] and between the drain electrode 31 and the semiconductor layer 33. [are also ohmic contacted]. A gate pad 15 and a source pad [25] 67, the terminals of the bus lines, are formed at the end portion of the gate line 13 and the source

line 23, respectively. Additionally, a gate pad terminal 57 and a source pad terminal [67] 25 are formed on the gate pad 15 and the source pad 67 [25], respectively.

Page 3, line 15:

As the signal voltage applied to the gate pad 15 is applied to the gate electrode 11 via the gate line 13, the TFT 19 of the [corresponded] corresponding gate electrode 11 [is in] transitions to the ON state. Then the source electrode 21 and the drain electrode 31 of the TFT 19 are electrically connected so that the electrical picture data applied to the source pad 25 is sent to the drain electrode [27] 31 through the source line 23 and the source electrode 21. Therefore, by controlling the signal voltage to the gate electrode 11, the transfer of picture data to the drain electrode is controlled. That is, the TFT 19 acts as a switching element. A gate insulating layer 17 is inserted between the layer including the gate electrode [13] 11 and the layer including the source electrode 23 to electrically isolate them. A passivation layer 37 is formed on the layer including the source line 23 to protect all elements of the transistor.

Page 4, line 18:

As shown in Fig. 3, the ACF 71 comprises a plurality of conductive ball 95 coated with an insulation membrane 93 in an isotropic film 31. On the pad terminals 47 connected to the pads 45 (for example, the gate pads 15 or the source pad [25] 67) at the edge of the liquid crystal panel, an ACF 71 is attached and TCP 73 is sequentially attached thereon. At this time, the conductive pad 75 of the TCP 73 should be aligned with the pad 45 (for example, the gate pads 15 or the source pad [25] 67) of the liquid crystal panel, as shown in Fig. 4a. The TCP 73 is pressed and heated while the conductive balls 95 are inserted between the TCP pad 75 and the pad terminal 47 of the liquid crystal panel. When sufficient pressure is applied against the TCP 73, the insulation membrane 93 covering the conductive ball 95 are broken so that [the] each TCP pad 75 [is] becomes electrically connected to each pad terminal 47 of the liquid crystal

panel, as shown in Fig. 4b. Even if there are some conductive balls 95 between the neighbored pad terminals 47, the neighbored pad terminals 47 are electrically isolated [to] from each other because the conductive balls 95 are covered by the insulation membrane 93.

Page 9, line 2:

Fig. 7 shows a plan view of an active panel according to a preferred embodiment of the present invention. On a transparent substrate 101, a first metal layer 211 is formed by depositing aluminum or aluminum alloy, as shown in Fig. 8a. A second metal layer 213 is formed by depositing a metal having a high melting point such as molybdenum, tantalum, tungsten or antimony sequentially on the first metal layer 211. These stacked metal layers 211 and 213 are patterned in a first mask process to form a gate electrode 111, a gate line 113 and a gate pad 115. Once these stacked layers 211 and 213 are patterned by a wet etching method, then the gate materials, such as the gate electrode, the gate line and the gate pad have a cross sectional shape [of which] where the width of the second metal layer 213 is narrower than that of the first metal layer 211. A plurality of the gate [line] lines 113 is arrayed and fabricated in a vertical direction. The gate electrode 111 is derived from the gate line 113 and disposed at a corner of the designed pixel. The gate pad 115 is disposed at the end of the gate line 113, as shown in Figs. 7 and 8a.

Page 9, line 20:

On the substrate having the gate material stacked with the first metal layer 211 and the second metal layer 213, an inorganic insulating material such as a silicon nitride [is deposited] or a silicon oxide is deposited or an organic insulating material such as BCB (benzocyclobutane) or acrylic resin is coated to form a gate 5 insulating layer 117. An intrinsic semiconductor material, such as a pure amorphous silicon, and an extrinsic semiconductor material, such as an impurity doped amorphous silicon, are sequentially deposited thereon. These stacked layers are patterned using a second mask process to form a semiconductor layer 133 and a doped semiconductor

layer 135. They are disposed on the gate insulating layer over the gate electrode 111, as shown in Figs. 7 and 8b.

Page 11, line 6:

On the passivation layer 137, a transparent conductive material such as ITO (Indium Tin Oxide) is deposited and patterned using a fifth mask process to preferably form a pixel electrode 141, a gate pad terminal 157 and a source pad terminal 167. The pixel electrode 141 connects to the drain electrode 131 through the drain contact hole 171. The gate pad terminal 157 connects to the gate pad 115 through the gate contact hole 151. The source pad terminal [157] 167 connects to the source pad 125 through the source contact hole 161, as shown in Figs. 7 and 8e.

In the Claims

Please amend the claims as follows:

12. (Amended) A method for manufacturing an active panel of a liquid crystal display device, comprising steps of:

providing a transparent substrate;

fabricating a plurality of gate and source lines above the transparent substrate, each line having a pad;

forming a first layer above the transparent substrate to cover at least a portion of the transparent substrate, wherein the first layer exposes the pad of the each line and defines at least one opening near the pad, the opening having a depth lower than the surface of the first layer; and

forming a second layer having a first part and a second part, wherein the first part is affixed to the pad to provide an electrical signal to the line and the second part is affixed to a bottom surface of the opening defined in the first layer to enhance adhesion between the first and second layers.